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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,798	12/31/2001	John M. Brown	1662-53900 (P01-3748)	2942

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CONLEY ROSE, P.C.
P. O. BOX 3267
HOUSTON, TX 77253-3267

EXAMINER	
AMIN, NIRAV S	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,798	BROWN ET AL.	
	Examiner	Art Unit	
	Nirav S Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 15* is/are rejected.

7)☒ Claim(s) *4-6,13,14 and 16-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 9 objected to because of the following informalities: It appears "circuit board" was meant to be "computer system". It is assumed that it is a "computer system". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Voit (US Patent No. 6,510,473) in view of Duncan et al. (US Patent No. 6,782,438) herein after referred to as Duncan.

As per claim 1, Voit discloses a computer (400) system comprising: a backplane that includes multiple sockets (308), a bus (312) that couples the multiples sockets (308) together, wherein the bus includes a capability signal line (M66EN) and a circuit board (309) inserted in one of the multiple sockets (308), and configured to limit a voltage on the capability signal line to one of two predetermined values, wherein the values are indicative of different bus component capability levels [Column 5, lines 3-10]. Voit does not disclose a circuit board (309) inserted in one of the multiple sockets (308), configured to limit a voltage on the capability signal line to one of three predetermined values. Duncan discloses a circuit (700) configured to limit a voltage to one of three

predetermined values (Figure 7C), wherein the values are indicative of different bus component capability levels [Column 7, lines 1-16] for the benefit of having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include circuit configured to limit a voltage to one of three predetermined values as taught by Duncan in the computer taught by Voit. The motivation for doing so would have been having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9].

As per claim 2, Voit discloses the predetermined values are indicative of a maximum bus clock rate supported by the circuit board [Column 5, lines 6-10].

As per claim 3, Voit discloses the circuit board includes a circuit that limits the voltage on the capability signal line when the circuit is enabled [Column 5, lines 32-34].

As per claim 8, Voit discloses the backplane further includes a circuit (108) to power the capability signal line (M66EN) at a voltage no higher than a predetermined voltage that is indicative of the capability level of the backplane [Column 5, lines 42-44].

As per claim 9, Voit discloses a computer system (400) including: a processor (304), a memory coupled to the processor (306), a bridge device (310) coupled between the processor and the backplane; and a long term storage device (406) coupled to the bridge device.

As per claim 10, Voit discloses, a processor (304), a memory coupled to the processor (306), a peripheral bus (312), a bridge device (310) coupled between the

processor (304) and the peripheral bus (312), and a long-term storage device (406), wherein the peripheral bus includes a capability signal line having a voltage that is one of two predetermined voltages each being indicative of a different bus capability level [Column 5, lines 3-10]. Voit does not disclose the capability signal line having one of three predetermined values. Duncan discloses a circuit (700) configured to limit a voltage to one of three predetermined values (Figure 7C), wherein the values are indicative of different bus component capability levels [Column 7, lines 1-16] for the benefit of having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include circuit configured to limit a voltage to one of three predetermined values as taught by Duncan in the computer taught by Voit. The motivation for doing so would have been having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9].

As per claim 11, one or more peripheral components (309) coupled to the peripheral bus (312), wherein each peripheral component is configured to limit the voltage on the capability signal line to a corresponding predetermined voltage that is indicative of a corresponding capability level of the peripheral component [Column 5, lines 6-10].

As per claim 12, Voit discloses the capability level is the maximum bus clock frequency supported by the peripheral component [Column 5, lines 6-10].

As per claim 15, Voit discloses a method of determining a maximum bus clock rate supported by various components [Column 3, lines 12-15], comprising of coupling the components (309) to a bus (312) having a capability signal line (M66EN), supplying electrical current to the capability signal line [Column 5, lines 32-34], wherein each of the components limits a voltage on the capability signal line to no more than a predetermined voltage that is indicative of a maximum bus clock rate supported by the component [Column 5, lines 3-10], each predetermined voltage being one of a set of two predetermined voltages that are indicative of different maximum clock rates and setting a bus clock rate to the maximum clock rate associated with the voltage on the capability signal line [Column 5, lines 6-10]. Voit does not disclose each predetermined voltage being one of a set of three predetermined voltages. Duncan discloses a circuit (700) configured to limit a voltage to one of three predetermined values (Figure 7C), wherein the values are indicative of different bus component capability levels [Column 7, lines 1-16] for the benefit of having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include circuit configured to limit a voltage to one of three predetermined values as taught by Duncan in the computer taught by Voit. The motivation for doing so would have been having a standard IO platform that is flexible enough to service the variety of devices demanded by a wide range of applications [Column 2, lines 7-9].

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Voit in view of Duncan as applied to claim 1 above, and further in view of Lee el al. (US Patent No. 5,678,065) herein after referred to as Lee.

Voit discloses multiple circuit boards inserted in corresponding sockets and configured to limit the voltage on the capability signal line to a predetermined value that is indicative of the capability level of the corresponding circuit board. Voit does not disclose the voltage on the capability signal line is determined by the circuit board having the lowest limit. Lee discloses a system wherein the voltage on the capability signal line is determined by the circuit board having the lowest voltage limit [Column 3, lines 23-32] to avoid bus malfunction [Column 2, lines 18-28]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the voltage on the capability signal line determined by the circuit board having the lowest limit. The motivation for doing so would have been to avoid bus malfunction [Column 2, lines 18-28].

Allowable Subject Matter

Claims 4, 5, 13, 14, 16, 18 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 4, the prior art fails to disclose or suggest the voting circuit includes a zener device configured to limit the voltage to less than a predetermined value that is indicative of the capability level of the circuit board.

Regarding claim 5, the prior art fails to disclose or suggest the circuit board further includes a sample circuit that latches a digital value indicative of the voltage on the capability signal line.

Regarding claim 13, the prior art fails to disclose or suggest that each of the peripheral components includes a voting circuit having a zener diode configured for a predetermined voltage corresponding to the capability level of the peripheral component.

Regarding claim 14, the prior art fails to disclose or suggest that each peripheral includes a voting circuit that limits the voltage on the capability signal line when a peripheral bus reset signal is asserted.

Regarding claim 16, the prior art fails to disclose or suggest asserting a bus reset signal while supplying electrical current to the capability signal line.

Regarding claim 18, the prior art fails to disclose or suggest the components include zener devices configured in accordance with the maximum bus clock rate supported by the components.

Regarding claim 22, the prior art fails to disclose or suggest preventing the newly added bus component from participating in bus transaction until the bus reset signal is next asserted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA

REHANA PERVEEN
PRIMARY EXAMINER
11-1-07